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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/541,645 | 07/06/2005 | Takeshi Honda | 19002 | 4090 |

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| EXAMINER | |
|---|---|
| LUU, PHO M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2824 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/28/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/541,645 | HONDA ET AL. | |
| | Examiner | Art Unit | |
| | Pho M. Luu | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *Preliminary amendment file on 7/6/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 4-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Search history*.

## DETAILED ACTION

1. Acknowledgment is made of applicant's Preliminary Amendment filed 06 July 2005. The changes and remarks disclosed therein were considered.

2. Claims 1-13 are pending in the application.

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Priority*

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

5. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 06 July 2005. The information disclosed therein was considered.

### *Drawings*

6. Figures 16-21 should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses the phrase **"The present invention relates to"** in page 32, line 2; **"The invention aims at shortening"** in page 32, lines 3-4 and **"The apparatus includes"** in page 32, line 6, which are implied. Correction is required. See MPEP § 608.01(b).

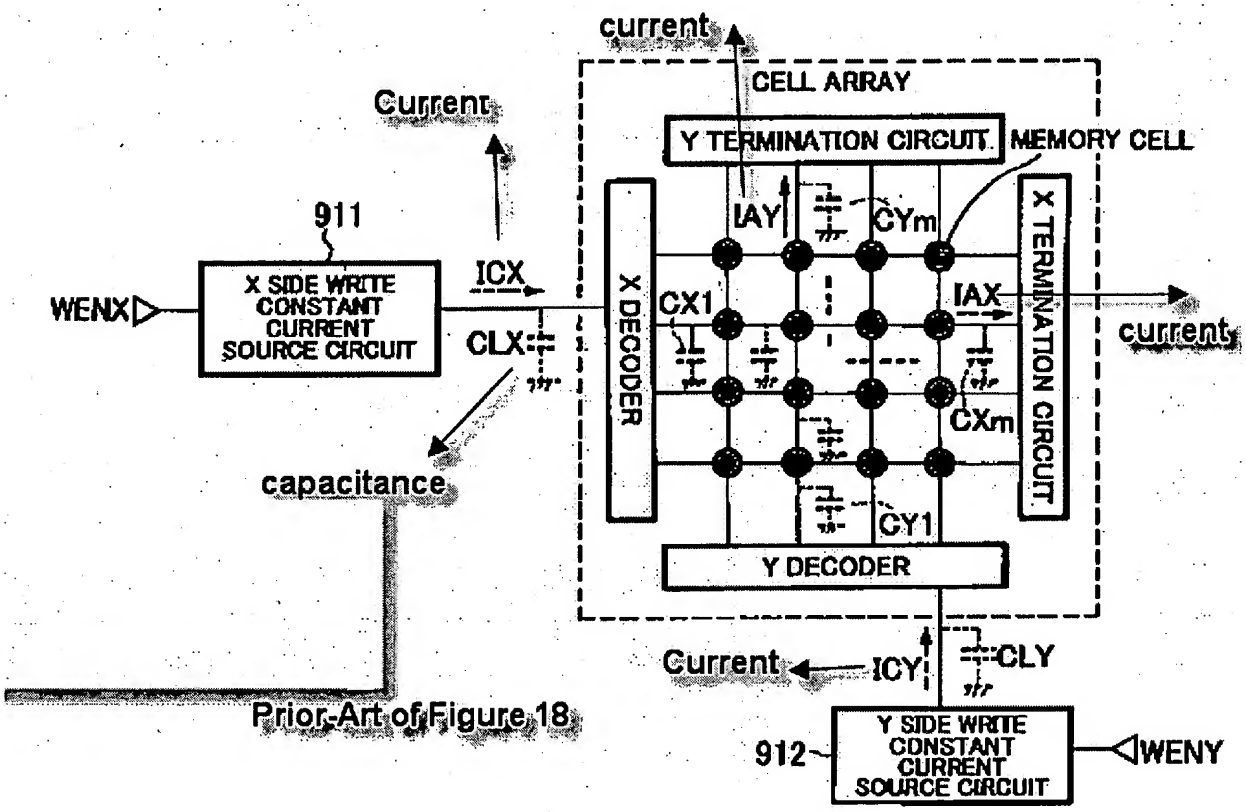
***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of Joo. (US. 6,762,970).

Regarding claim 1, Admission in Figure 18 discloses a semiconductor memory device **(MRAM, paragraph 0002, line 5)** comprising:




a storage element **(memory cell)** for storing information;

a constant current source **(constant current source circuits 911, 912)** for writing information into the storage element by flowing current **(current flows ICX, ICY) for example, constant current source circuits 911, 912 provide a constant currents output ICX, ICY flow to memory cells through the capacitor CLX, CLY and X-DECODER, Y-DECODER, respectively)** at a time when an amount of a current flowed **(current flow ICX, ICY)** by the constant current source reaches an amount of a current required to write information into the storage element at a predetermined position related to the storage element **(for example, a constant current ICX, ICY**

**output form the constant current source 911, 912 flows in the array of memory cell through the capacitor CLX, CLY for select memory cell, paragraph 0016).**

Admission does not discloses a boost circuit for charging parasitic capacitors at a time when an amount of a current flowed the constant current source reaches an amount of a current required to write information into the storage element at a predetermined position related to the storage element.

Joo in Figures 1 and 3 discloses a boost circuit **(with 11 in Figure 1; and 21 in Figure 3)**

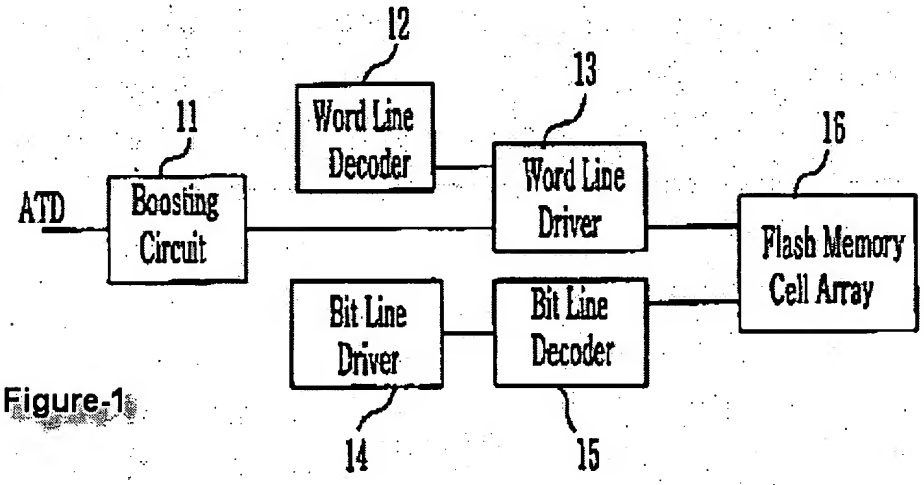



Figure 1

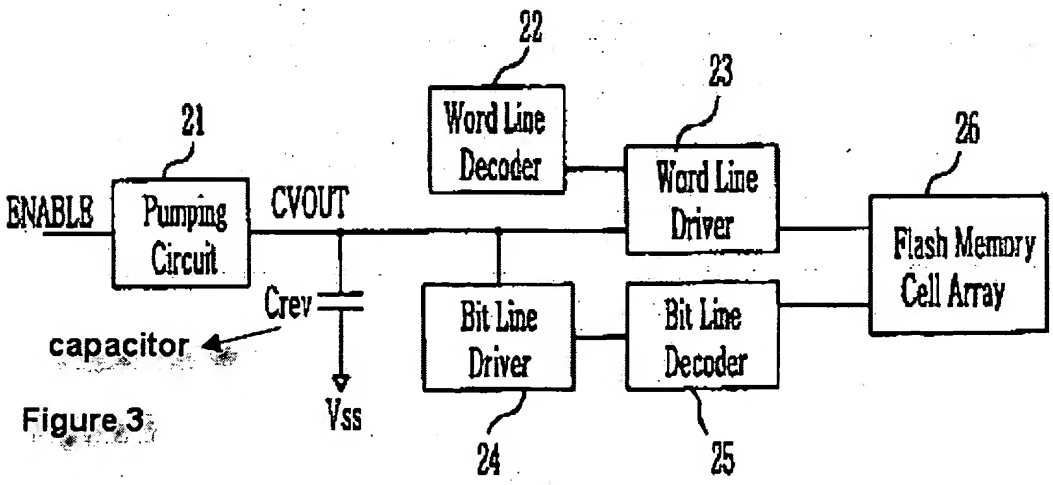



Figure 3

for charging parasitic capacitors **(pump circuit 21 charge a capacitor Crev, Figure 3, column 3, lines 10-11)** when an amount of a current flowed the constant current source reaches an amount of a current required to write information into the storage element (select memory cell) **(for example, the reference of Joo in Figure 3 show that pump circuit 21 to generate the output voltage CVOUT coupled to flash memory 26 and it is inherent that the output voltage CVOUT provide the constant current to select cell (store information of memory cell) of flash memory array 26 through the word line driver 23, see column 3, lines 7-13 and lines 21-24)**.

Since Admission and Joo are analogous art because they are form the same fielded endeavor; semiconductor device.

It would have been obvious to one or ordinary sill in the art at the time of the invention was made to a person having ordinary skill in the art to apply the Joo means of boosting circuit in charge parasitic capacitor to the device of Admission, for the purpose of reduce the area without a boosting pump circuit occupying a large area and also reduce the power consumption by the edge trigger included in the charge pump circuit **(column 5, lines 5-11)**.

Regarding claim 3, Joo in Figures 1 and 3 discloses the semiconductor memory device that the boost circuit **(11, Figure 1 and 21, Figure 3)** comprising a condenser for storing charge to charge the parasitic capacitor **(a parasitic capacitor Cres is a condenser, for example, by definition of capacitor, the capacitor is an electric circuit element used to store charge temporarily, consisting in general of two metallic plates separated and insulated from each other by a dielectric that called *condenser*)**.

***Allowable Subject Matter***

10. Claims 2 and 4-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the prior art of record do not disclose or suggest that the predetermined position is a position, which is a current, generates a magnetic field applied to the tunnel magneto-resistance element.

Regarding claim 4, the prior art of record do not disclose or suggest that the circuit for setting a voltage between both electrodes of the condenser to a voltage greater than a power supply voltage.

Regarding claim 5-10, the prior art of record do not disclose or suggest that the boost circuit comprises switching means for selecting one or more condenser to be used for charging to an amount of charge required to charge the parasitic capacitor

Regarding claim 11, the prior art of record do not disclose or suggest that the returning at least a part of charge on parasitic capacitors which are present on a current path of a current for writing information into the storage element to a node where charge of the boost circuit is stored.

Regarding claim 12, the prior art of record do not disclose or suggest that the boost circuit is set at a time after completion of an operation period of the constant current source.

Regarding claim 13, the prior art of record do not disclose or suggest that the retaining a part of charge on parasitic capacitors which are present on a current path of a current for writing information into the storage element in dependence on history of an operation node, so as to suppress discharge of the boost circuit.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 571.273.8300 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
14 March 2007. pml

Pho Miner Luu
Art Unit. 2824.
Patent Examiner.